The University of Sydney

School of Electrical and Information Engineering

James G Rathmell (jimr@ee.usyd.edu.au)

Tutorial 5: Computer Components - Memory Interface

1 Introduction

This tutorial gives you experience in interfacing memory devices to a CPU. It builds upon the LCD interface completed in Tutorial 4 by adding a number of memory devices to the CPU. The LCD display can be used for display of diagnostic information when testing the memory interface.

Before attempting this tutorial, Tutorial 4 must be completed using the solution provided on the ELEC4605 web site. Then, the Tutorial 4 solution can be modified into a hierarchy, in keeping with the principles of Digital Systems Designs. This includes moving the address decoding into a separate module. Finally, the memory devices will be added. This also requires the addition of a data-bus multiplexer to direct data back to the CPU core.

Read through the complete tutorial exercise first to understand what the final outcome should be. The final top-level design is shown in Figure 4. Don't be too concerned if you are unable to complete the tutorial as some of the material covered in this tutorial exercise will be repeated for the laboratory project.

2 Complete Tutorial 4 Exercise

The solution to Tutorial 4 is on the ELEC4605 web site. If you have not already completed the first exercise from Tutorial 4, do this now as Tutorial 5 will build upon it.

3 Design Hierarchy

The solution from Tutorial 4 has the complete design on one schematic. It is good practice to divide a design into a number of functional modules in the form of a hierarchy as covered in the Digital Systems Design topic in lectures.

Copy your solution from Tutorial 4 into another directory to complete the Tutorial 5 exercise. Change the design by moving the LCD interface onto another schematic. This schematic should look like that shown in Figure 1. The VHDL

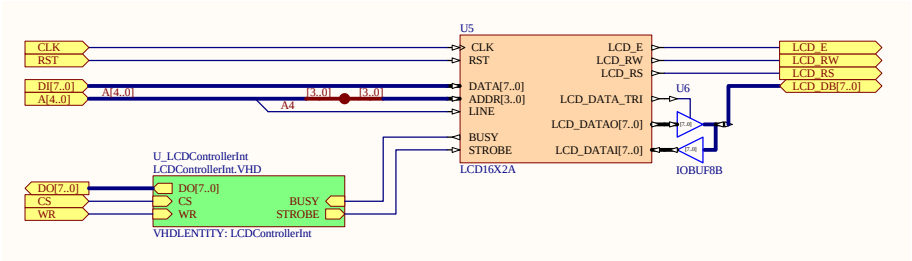

Figure 1: The LCD interface schematic.

code for the LCD interface also has to be changed to use a chip select input rather than decoding the address lines. The **BUSY** signal can also be connected directly to **DO0** without the need to use the **MEMRD** signal (done in the VHDL code).

A separate VHDL symbol must be added to the top level that takes in the address lines and generates a chip select output for the LCD display. To make decoding easier, make the chip select line active for a 1K block starting at `0x0000`. The

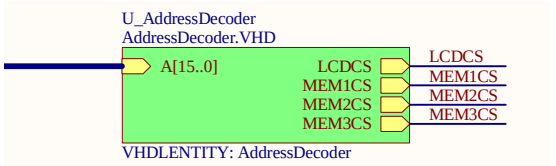

Figure 2: Address decoder used to select the devices connected to the CPU.

symbol for the decoder is shown in Figure 2. Note that it also shows chip select outputs used for the memory devices which will be added later.

The test program used in Tutorial 4 should be used to check that the design is working correctly. You should also simulate the VHDL code for the LCD interface and the address decoder to check for correct operation.

4 Add Memory Devices

The final task is to add three 1K memory devices to the design starting at address `0x8000`. Use the RAMSE_8x1K components. This is similar to the device used for the program memory but it also has an enable signal. To write to the memory, the enable signal must also be asserted otherwise the write-enable signal will have no effect. The enable signal uses positive logic (even though the documentation suggests otherwise).

First modify the address decoder to include the three chip-select signals used to select the memory devices for the address ranges mentioned above. Test that the chip-select signals for the memory devices work as expected.

As there are now four devices connected to the CPU (the LCD display and the three memory devices) it is not possible to connect all the data output signals back to the CPU. Instead a data-bus multiplexer must be used to select one data source which will be connected back to the CPU. Implement this data-bus multiplexer in VHDL. The symbol is shown in Figure 3. You should also simulate the data-bus multiplexer to ensure correct operation.

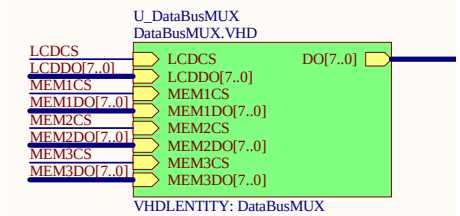

Figure 3: Data-bus multiplexer to select which data lines are connected to the CPU.

Another method for connecting data signals back to the CPU will be used for the laboratory project. This will highlight that there are a number of ways in which a design can be decomposed.

5 Write Test Program

Write a test program to check that the memory devices are working correctly. You can use the LCD display for displaying diagnostic messages.

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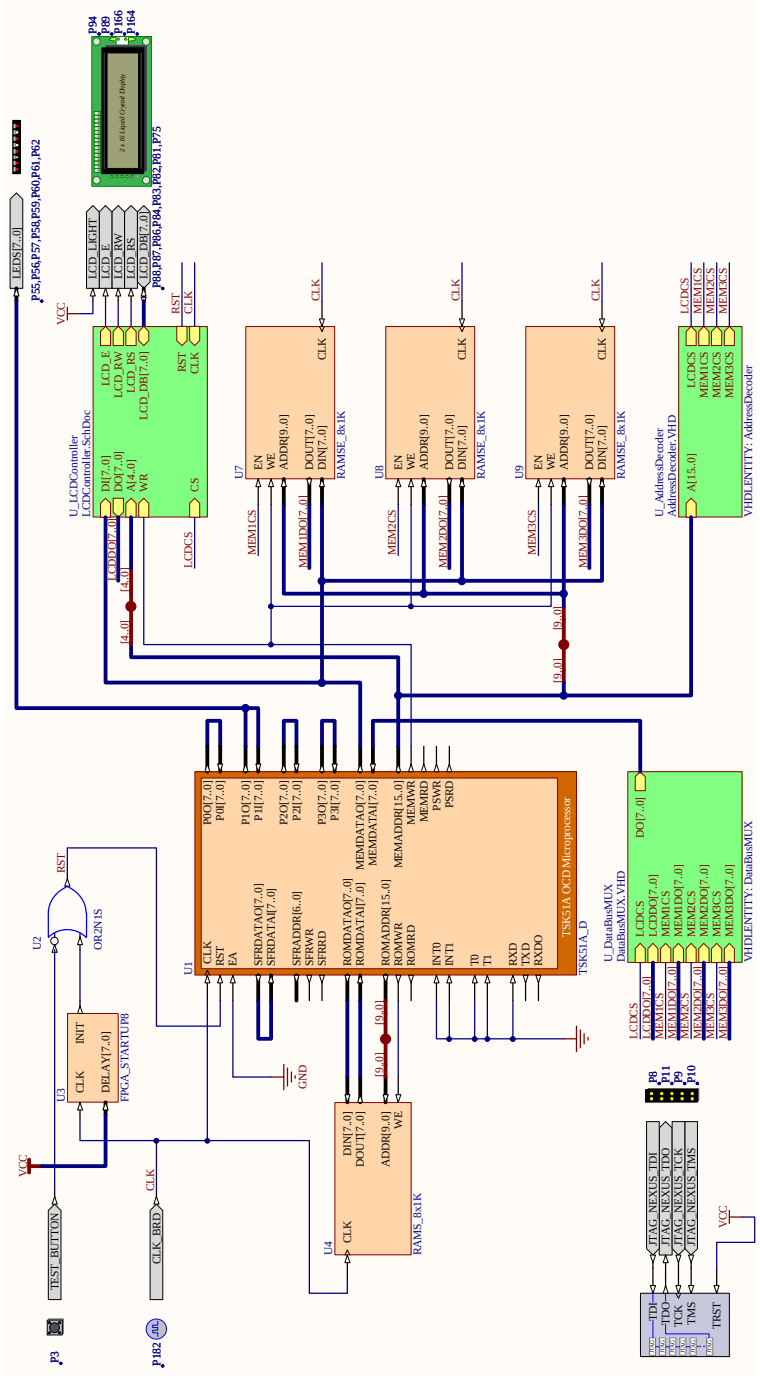

Figure 4: Complete design containing LCD display and three extra memory devices.