

Figure 2: Address decoder used to select the devices connected to the CPU.

symbol for the decoder is shown in Figure 2. Note that it also shows chip select outputs used for the memory devices which will be added later.

The test program used in Tutorial 4 should be used to check that the design is working correctly. You should also simulate the VHDL code for the LCD interface and the address decoder to check for correct operation.

4 Add Memory Devices

The final task is to add three 1K memory devices to the design starting at address 0×8000 . Use the RAMSE_8x1K components. This is similar to the device used for the program memory but it also has an enable signal. To write to the memory, the enable signal must also be asserted otherwise the write-enable signal will have no effect. The enable signal uses positive logic (even though the documentation suggests otherwise).

First modify the address decoder to include the three chip-select signals used to select the memory devices for the address ranges mentioned above. Test that the chip-select signals for the memory devices work as expected.

As there are now four devices connected to the CPU (the LCD display and the three memory devices) it is not possible to connect all the data output signals back to the CPU. Instead a data-bus multiplexer must be used to select one data source which will be connected back to the CPU. Implement this data-bus multiplexer in VHDL. The symbol is shown in Figure 3. You should also simulate the data-bus multiplexer to ensure correct operation.

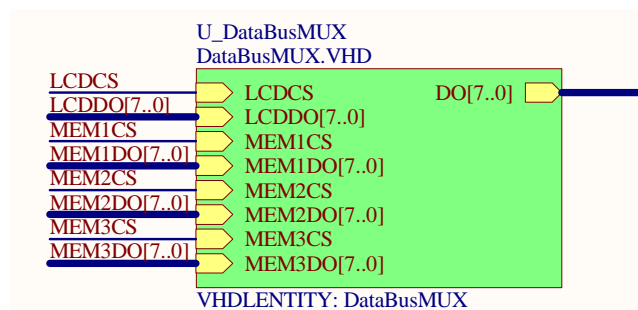


Figure 3: Data-bus multiplexer to select which data lines are connected to the CPU.

Another method for connecting data signals back to the CPU will be used for the laboratory project. This will highlight that there are a number of ways in which a design can be decomposed.

5 Write Test Program

Write a test program to check that the memory devices are working correctly. You can use the LCD display for displaying diagnostic messages.

