FPGAs
Most electronics rely on application-specific ICs (ASICs) for perf, cost and P

Source: Arvind MIT
A generalised integrated circuit
- Logic blocks for digital operations
- Programmable interconnect for routing

Arbitrary digital circuits can be implemented

Functionality downloaded to FPGA memory (in seconds)

Source: Steve Wilton (UBC)
FPGA Embedded Blocks

Source: Xilinx

Hard IP blocks for widely-used functions: faster, more efficient, lower power
Careful choice: every user must pay for these functions, whether used or not

Source: Xilinx
Zynq (ARM+ Reconfigurable Fabric)

Source: Xilinx
Xilinx 7-series FPGAs, 28nm

<table>
<thead>
<tr>
<th>Feature</th>
<th>740</th>
<th>1,920</th>
<th>3,600</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Slices</td>
<td>740</td>
<td>1,920</td>
<td>3,600</td>
</tr>
<tr>
<td>DSP Performance (symmetric FIR)</td>
<td>930GMACs</td>
<td>2,845GMACs</td>
<td>5,335GMACs</td>
</tr>
<tr>
<td>Transceiver Count</td>
<td>16</td>
<td>32</td>
<td>96</td>
</tr>
<tr>
<td>Transceiver Speed</td>
<td>6.6Gb/s</td>
<td>12.5Gb/s</td>
<td>28.05Gb/s</td>
</tr>
<tr>
<td>Total Transceiver Bandwidth (full duplex)</td>
<td>211Gb/s</td>
<td>800Gb/s</td>
<td>2,784Gb/s</td>
</tr>
<tr>
<td>Memory Interface (DDR3)</td>
<td>1,066Mb/s</td>
<td>1,866Mb/s</td>
<td>1,866Mb/s</td>
</tr>
<tr>
<td>PCI Express® Interface</td>
<td>x4 Gen2</td>
<td>x8 Gen2</td>
<td>x8 Gen3</td>
</tr>
<tr>
<td>Analog Mixed Signal (AMS)/XADC</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Configuration AES</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>I/O Pins</td>
<td>500</td>
<td>500</td>
<td>1,200</td>
</tr>
</tbody>
</table>

Source: Xilinx
ASIC vs FPGA Cost

Crossover volume increases with decreasing feature size.
ASIC Development Costs

Drives Fewer ASIC Design Starts

ASIC Design Starts Lag Moore’s Law;

500Ku* @ 0.5u

27Mu* @ 65nm

>50Mu* @ 22nm

Primary Node for ASICs 130nm remains the primary process node for ASIC design starts from 2003 to 2010

Source: Altera
## Return on Investment Analysis

### ASIC / ASSP (65nm) Development Cost
- **$55M**

### 20% of Revenue on R&D
- **Revenue Target: $275M**

### $10 to $50 Device ASP

### Unit Volume Req’d
- **5Mu to 27Mu**

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**Very Few High Volume Applications Justify ASIC / ASSP Development**

Source: Altera
Application Domains

End Market Weight (% of Revenue in 2009)

Relative Growth Potential
(3 to 5 Year Horizon)

Larger

Higher

- Telecom & Wireless
- Other
- Networking, Computer & Storage
- Industrial Automation
- Military
- Automotive

Source: Altera
Typical High Performance Commercial Applications

Application
- Optical Transport OTU Transponder
- 40GbE/100GbE Switch
- Radar

Requirements
- >350 MHz performance
- 28 Gbps transceivers
- 10GBASE-KR backplane support
- High-performance on-chip memory
- High-performance and flexible memory controller
- Hard system-level IP for bandwidth
- High precision DSP

Solution

Process: 28HP
- >350 MHz performance
- Lowest power in its class
- Up to 1.1M LEs on a monolithic die

Transceiver: 14.1 Gbps/28 Gbps

Product Architecture:
- Soft memory controller supports 800MHz DDR3 DIMM
- 2,560 M20K memory blocks
- 54x54 variable precision DSP

System IP:
- PCIe Gen3 x8, 40 GbE/100 GbE, Interlaken

Source: Altera
Architectural Choices

General-purpose processor

Application-specific processor

Dedicated accelerators

Reconfigurable processor

Source: Rabaey UCB
Approximately three orders of magnitude in inefficiency from general-purpose to dedicated!
FPGA vs DSP and CPU Cost Comparison

Berkeley BEE2 cost comparison (FPGA, DSP1, DSP2, uP)

- XC2VP70
- C6415-7E
- C6415T-1G
- Pentium 4-3.8 GHz

MMACs/s/dollar

Spectrometer, PFB, Correlator
Traditionally designed using ASIC development tools
- VHDL/Verilog very low level
- Chisel is a recent tool which is higher level

Recent advances
- Vivado HLS
- OpenCL

Extensive module generators and libraries e.g. filters, fft, floating-point, maths coprocessors, soft processors, network controllers, memory controllers, I/O controllers …

Still an active research topic
Comparison of FPGAs with uP and ASIC

- Compared with uP and DSP
  - higher speed, lower power, smaller variance in execution time
  - Longer development times, higher cost per unit

- Compared with ASICs
  - Lower initial cost

- Rides Moore’s Law, development costs amortised over users
  - Faster time to market, lower risk
  - Can be customised to problem in ways not possible with ASICs