Case Study: Xilinx FPGAs
7 Series FPGA Overview

Source of slides that follow: Xilinx
# 7 Series FPGA Families

<table>
<thead>
<tr>
<th>Maximum Capability</th>
<th>ARTIX.™️</th>
<th>KINTEX.™️</th>
<th>VIRTEX.™️</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lowest Power and Cost</td>
<td>20K – 355K</td>
<td>70K – 480K</td>
<td>285K – 2,000K</td>
</tr>
<tr>
<td>Block RAM</td>
<td>12 Mb</td>
<td>34 Mb</td>
<td>65 Mb</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>40 – 700</td>
<td>240 – 1,920</td>
<td>700 – 3,960</td>
</tr>
<tr>
<td>Peak DSP Perf.</td>
<td>504 GMACS</td>
<td>2,450 GMACs</td>
<td>5,053 GMACs</td>
</tr>
<tr>
<td>Transceivers</td>
<td>4</td>
<td>32</td>
<td>88</td>
</tr>
<tr>
<td>Transceiver Performance</td>
<td>3.75Gbps</td>
<td>6.6Gbps and 12.5Gbps</td>
<td>12.5Gbps, 13.1Gbps and 28Gbps</td>
</tr>
<tr>
<td>Memory Performance</td>
<td>1066Mbps</td>
<td>1866Mbps</td>
<td>1866Mbps</td>
</tr>
<tr>
<td>I/O Pins</td>
<td>450</td>
<td>500</td>
<td>1,200</td>
</tr>
<tr>
<td>I/O Voltages</td>
<td>3.3V and below</td>
<td>3.3V and below</td>
<td>3.3V and below</td>
</tr>
</tbody>
</table>

Source: Xilinx
The Virtex-7 family has several devices:

- **Virtex-7**: General logic
- **Virtex-7XT**: Rich DSP and block RAM, higher serial bandwidth
- **Virtex-7HT**: Highest serial bandwidth

Source: Xilinx
Common elements enable easy IP reuse for quick design portability across all 7 series families
- Design scalability from low-cost to high-performance
- Expanded eco-system support
- Quickest TTM

- **Logic Fabric**
  - LUT-6 CLB
- **On-Chip Memory**
  - 36Kbit/18Kbit Block RAM
- **DSP Engines**
  - DSP48E1 Slices
- **Hi-performance Serial I/O Connectivity**
  - Transceiver Technology
- **Precise, Low Jitter Clocking**
  - MMCMs
- **Enhanced Connectivity**
  - PCIe® Interface Blocks
- **Hi-perf. Parallel I/O Connectivity**
  - SelectIO™ Technology

Source: Xilinx
Fourth-Generation ASMBL Architecture

- **Optimized FPGA feature mix for different families/members**
  - FPGA comprises columns of different resources
    - Clocking, I/O, BRAM, DSP, HSSIO

- Enables the unified architecture between the different 7 series families

- Enables different resource ratios within the different devices

CMT = clock management tile, HSSIO = high speed serial I/O

Source: Xilinx
Two side-by-side slices per CLB
- Slice_M are memory-capable
- Slice_L are logic and carry only

Four 6-input LUTs per slice
- Consistent with previous architectures
- Single LUT in Slice_M can be a 32-bit shift register or 64 x 1 RAM

Two flip-flops per LUT
- Excellent for heavily pipelined designs
36K/18K block RAM
- All Xilinx 7 series FPGA families use same block RAM as Virtex-6 FPGAs

Configurations same as Virtex-6 FPGAs
- 32k x 1 to 512 x 72 in one 36K block
- Simple dual-port and true dual-port configurations
- Built-in FIFO logic
- 64-bit error correction coding per 36K block
- Adjacent blocks combine to 64K x 1 without extra logic

Source: Xilinx
All 7 series FPGAs share the same DSP slice:
- 25x18 multiplier
- 25-bit pre-adder
- Flexible pipeline
- Cascade in and out
- Carry in and out
- 96-bit MACC
- SIMD support
- 48-bit ALU
- Pattern detect
- 17-bit shifter
- Dynamic operation (cycle by cycle)

Source: Xilinx
Based on the established Virtex-6 FPGA clocking structure
- All 7 series FPGAs use the same unified architecture

Low-skew clock distribution
- Combination of paths for driving clock signals to and from different locations

Clock buffers
- High fanout buffers for connecting clock signals to the various routing resources

Clock regions
- Device divided into clock regions with dedicated resources

Clock management tile (CMT)
- One MMCM and one PLL per CMT
- Up to 24 CMTs per device

MMCM = mixed mode clock manager

Source: Xilinx
Two distinct I/O types
- High range: Supports standards up to 3.3V
- High performance: Higher performance with more I/O delay capability
- Supports I/O standards up to 1.8V

Extension of logic layer functionality
- Wider input/output SERDES
- Addition of independent ODELAY

New hardware blocks to address highest I/O performance
- Phaser, IO FIFO, IO PLL

Source: Xilinx
Stacked Silicon Interconnect Technology

- Largest Virtex-7 device is almost three times the size of the largest Virtex-6 device
  - Growth is higher than Moore’s Law dictates

- Enabled by Stacked Silicon Interconnect (SSI) technology
  - Multiple FPGA die on a silicon interposer
  - Each die is referred to as a Super Logic Region (SLR)
  - Vast quantity of interconnect between adjacent SLRs are provided by the interposer

Source: Xilinx
Stacked Silicon Implications

- Enables substantially larger devices
- Device is treated as a single monolithic device
  - Tool chains place and route complete device as if it was one die
- Minor design considerations around clocking and routing

Source: Xilinx

TSV=through silicon via, c4=controlled collapse chip connection
High-Speed Serial I/O Transceivers

- Available in all families
- GTP transceivers – up to 3.75 Gbps
  - Ultra high volume transceiver
  - Wire bond package capable
- GTX transceivers – up to 12.5 Gbps
  - Support for the most common 10 Gbps protocols
- GTH transceivers – up to 13.1 Gbps
  - Support for 10 Gbps protocols with high forward error correction overhead
- GTZ transceivers – up to 28 Gbps
  - Enables next generation 100–400Gbps system line cards

Source: Xilinx
Features
- Compliant to PCIe Revision 2.1
- Endpoint & root port
- AXI user interface
- <100 ms configuration*
- FPGA configuration over PCI Express*
- End-to-end CRC*
- Advanced error reporting*
- 100-MHz clocking

New wrappers
- Multi-function*
- Single-root I/O virtualization*

Configurations
- Lane widths: x1-8
- Data rates: Gen1 & Gen2 (2.5/5.0 Gbps)
- Dependent on GT and fabric speed

*New features in 7 series

Source: Xilinx
XADC: Dual 12-Bit 1-MSPS ADCs

- 17 External Analog Inputs
- On-Chip Sensors Supplies ±1% Temperature ±4°C
- On-Chip Sensors
- ADC 1: 2 x 12 Bits 1 MSPS
- ADC 2: 2 x 12 Bits 1 MSPS
- MUX
- Arbitrator
- DRP
- Dynamic Reconfiguration Port
- Interconnect
- JTAG
- ADC Results
- Status Registers
- Control Registers
- Define XADC Operation
- Initialize with Attributes

Source: Xilinx
The different families in the 7 series provide solutions to address the different price/performance/power requirements of the FPGA market

- Artix-7 family: Lowest price and power for high volume and consumer applications
  - Battery powered devices, automotive, commercial digital cameras
- Kintex-7 family: Best price/performance
  - Wireless and wired communication, medical, broadcast
- Virtex-7 family: Highest performance and capacity
  - High-end wired communication, test and measurement, advanced RADAR, high performance computing

Source: Xilinx
Each 7 series I/O bank contains one type of I/O
- High (voltage) Range (HR)
- High Performance (HP)

Different devices have different mixtures of I/O banks

<table>
<thead>
<tr>
<th>I/O Types</th>
<th>Artix-7 Family</th>
<th>Kintex-7 Family</th>
<th>Virtex-7 Family</th>
<th>Virtex-7 XT/HT Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Range</td>
<td>All</td>
<td>Most</td>
<td>Some</td>
<td></td>
</tr>
<tr>
<td>High Performance</td>
<td>Some</td>
<td>Most</td>
<td>All</td>
<td></td>
</tr>
</tbody>
</table>

Source: Xilinx
Different families have different MGT devices

- Artix-7 family: GTP
- Kintex-7/Virtex-7 family: GTX
- Virtex-7 XT family: Mixture of GTX and GTH
- Virtex-7 HT family: Mixture of GTH and GTZ

<table>
<thead>
<tr>
<th>Speed Grade</th>
<th>Artix GTP</th>
<th>Kintex GTX</th>
<th>Virtex GTX</th>
<th>Virtex GTH</th>
<th>Virtex GTZ</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min</td>
<td>max</td>
<td>min</td>
<td>max</td>
<td>max (FF)</td>
</tr>
<tr>
<td>1LC/I</td>
<td>0.612</td>
<td>3.125</td>
<td>0.612</td>
<td>5.0</td>
<td>6.6</td>
</tr>
<tr>
<td>1C/I</td>
<td>0.612</td>
<td>3.125</td>
<td>0.612</td>
<td>5.0</td>
<td>6.6</td>
</tr>
<tr>
<td>2C/I</td>
<td>0.612</td>
<td>3.75</td>
<td>0.612</td>
<td>6.6</td>
<td>10.3125</td>
</tr>
<tr>
<td>3C</td>
<td>N/A</td>
<td>N/A</td>
<td>0.612</td>
<td>6.6</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Source: Xilinx
Packaging – Artix-7 Family

- Ultra low-cost wire bond technology
- Small form factor
- Fourth generation sparse chevron pin pattern
- Speeds up to 1.066 Gbps for parallel I/O
- Speeds up to 3.75 Gbps for MGT

Source: Xilinx
Kintex-7 devices are available in two different packages:
- Low cost bare die flip chip (FB) and conventional flip chip (FF)
- Small form factor packaging available

Fourth generation sparse chevron pin pattern

Speeds up to 2.133 Gbps for parallel I/O

Speeds up to 12.5 Gbps for MGT in FF package, and 6.6 Gbps in FB package

FB package has discrete substrate decoupling capacitors for MGT power supplies

Source: Xilinx
Packaging – Virtex-7 Family

- High performance flip chip (FF) package
- Fourth generation sparse chevron pin pattern
- Speeds up to 2.133 Gbps for parallel I/O
- Speeds up to 28.05 Gbps for MGT
- Discrete substrate decoupling capacitors:
  - MGT power supplies
  - Block RAM power supplies
  - I/O pre-driver power supplies

Source: Xilinx
Hard blocks needed for performance, power and low area

Different types of FPGAs have different features to address FPGA market

- Artix-7 family: Lowest price and power
- Kintex-7 family: Best price/performance
- Virtex-7 family: Highest performance/capacity

Source: Xilinx