Altera NIOS Processor
NIOS II Classic is a soft processor from Altera
- Has floating point, MMU, caching,
- Uses the Avalon bus
- Excellent supporting tools
- SOPC Builder generates designs from parameters such as data width, address range

Describe Avalon to External Bus Bridge
A NIOS II System

Source: Altera
Avalon to External Bus Bridge

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› Address—kbits (up to 32).
› BusEnable—1bit. Indicates that all other signals are valid, and a data transfer should occur.
› RW—1bit. Read(1), Write(0)
› ByteEnable — 16, 8, 4, 2 or 1 bits. Each bit indicates whether or not the corresponding byte should be read or written. These signals are active high.
› WriteData — 128, 64, 32, 16 or 8 bits. The data to be written to the peripheral device during a Write transfer.
› Acknowledge — 1 bit. Used by the peripheral device to indicate that it has completed the data transfer.
› ReadData—128, 64, 32,16. Data read from peripheral during a Read transfer.
› IRQ—1bit.Used by peripheral device to interrupt the processor.
Other Features

- Synchronous bus – all transfers occur on rising edge of clock
- Bus has time out
An Interface

Source: Altera
Timing Diagram

- Clock
- Address
- BusEnable
- R/W
- ByteEnable
- WriteData
- Acknowledge
- ReadData

Source: Altera
http://wl.altera.com/literature/lit-nio2.jsp